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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,324	10/25/2001	Richard H. Lawrence	42P11726	3859
8791	7590	08/31/2004	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			AMIN, NIRAV S	
			ART UNIT	PAPER NUMBER
			2115	

DATE MAILED: 08/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,324	LAWRENCE, RICHARD H.	
	Examiner	Art Unit	
	Nirav Amin	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10/25/2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 October 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>10/25/2001</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: Reference numbers 300 and 400 are not described in the specification. On page 4, line 22, and page 5, line 1 serial numbers for cited applications are missing. On page 9, line 6, "personal digital cellular(PCS)", appears to have the wrong acronym. On page 10, line 18, "a microprocessor, and memory, peripherals, a microprocessor, memory, and peripherals", microprocessor, memory and peripherals are listed twice.

Appropriate correction is required.

Claim Objections

Claim 12 objected to because of the following informalities: On line 8, it appears that "frequenc" was meant to be "frequency". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Schutz et al. (US Patent No. 5,440,520), herein after referred to as Schutz.

As per claim 7, Schutz discloses an article comprising: a storage medium [Figure 1A(20)] having stored thereon instructions, that, when executed by a computing platform, result in execution of adjusting a supply voltage to a system's processor

[Figure 3(50)] by: sensing the system processor's temperature [Figure 3(54)]; storing a plurality of acceptably low supply voltages [Column 6, lines 64-68] based at least in part on the processors sensed temperature and the processor's sensed clock frequency; and generating a command [Figure 3(58)] to adjust the system's supply voltage to approximately the acceptably low supply voltage.

As per claim 8, Schutz discloses storing of the plurality of acceptably low supply voltages comprises writing the acceptably low supply voltage to a flash memory [Column 7, lines 25-30].

As per claim 9, Schutz discloses generating of a command comprises transmitting the command from the system processor to a power source [Column 3, lines 59-62, Figure 1].

As per claim 10, Schutz discloses generating of a command comprises transmitting the command from a power controller to a power source [Column 3, lines 59-62, Figure 4].

As per claim 11, Schutz discloses a system comprising a personal computer [Column 1, lines 37-43].

Claims 12, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Dischler et al. (EP 712,064 A1), herein after referred to as Dischler.

As per claim 12, a method of adjusting a voltage level to a processor comprising: sensing a temperature and a clock frequency of the processor [Column 3, lines 1-4]; comparing the processor's sensed temperature and the processor's clock frequency to a table of data of an acceptably low voltage level for a plurality of processor's sensed

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temperatures and processor's sensed clock frequencies [Column 8, lines 33-38]; adjusting the voltage level of the processor to the acceptably low voltage level based at least in part on the processor's sensed temperature and the processor's sensed clock frequency [Column 3, lines 1-4].

As per claim 14, Dischler discloses adjusting the voltage level comprising of generating a set voltage command [Column 9, lines 16-18].

As per claim 15, Dischler discloses generating the set voltage command comprising of transmitting the set voltage command to a power source [Column 11, lines 3-12].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michail et al (Patent number: 6,119,241), herein after referred to as Michail, in view of Schutz.

As per claim 1, Michail discloses a processor [Column 2, lines 28-29] with an adjustable supply voltage [Column 2, line 36]; At least one temperature sensor, coupled to the processor to sense a temperature of the processor [Column 2, line 54]; The system to adjust the processor's supply voltage to an acceptably low supply voltage based at least in part on the processor's sensed temperature and a sensed clock

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frequency of the processor [Column 2, lines 28-37, Figure 1(500)]; Michail does not disclose expressly a flash memory to store a plurality of the acceptably low supply voltages for the processor. Schutz teaches a flash memory to store a plurality of the acceptably low supply voltages for the processor based at least in part on the processor's sensed clock frequency and the processor's sensed temperature [Column 4, lines 62-67, Figure 1a(20)] to increase circuit performance by avoiding speed limiting voltage/temperature combinations [Column 6, lines 35-37]. Michail and Schutz are analogous art because they are from the same field of endeavor of reduction of power consumption in integrated circuits. At the time of the invention it would have been obvious to a person of ordinary skill in the art to add flash memory to store a plurality of supply voltages, as taught by Schutz to the microprocessor as taught by Michail. The motivation for doing so would have been to increase circuit performance by avoiding speed limiting voltage/temperature combinations [Column 6, lines 35-37].

As per claim 2, Michail discloses the system coupled to a power source integrated with a power controller [Column 6, lines 5-7].

As per claim 3, Michail discloses the temperature sensor is integrated with the processor [Column 6, lines 39-41, Figure 4(58)].

As per claim 4, Michail discloses the temperature sensor attached to a ceramic package of the processor [Column 6, lines 40-41]. Although it is not expressly disclosed that the sensor is attached to the ceramic package, it would necessarily follow that if the sensor is "on chip", it would have to be on the package.

As per claim 5, Michail does not address the location of the temperature sensor. However, given the size of processors and the fact that the temperature sensor is on the ceramic package the distance between the temperature sensor and the processor would necessarily fall within the range of zero to seven centimeters.

As per claim 6, Michail discloses the system comprising a personal computer [Column 1, lines 8-11].

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dischler in view of Schutz.


Dischler discloses all the limitations of claim 12 as discussed in the rejection of claim 12. As per claim 13, Dischler does not expressly disclose storing the table of data in a flash memory. Schutz teaches storing the table of data in a flash memory [Column 7, lines 24-30] to increase circuit performance by avoiding speed limiting voltage/temperature combinations [Column 6, lines 35-37]. Dischler and Schutz are analogous art because they are from the same field of endeavor of reduction of power consumption in integrated circuits. At the time of the invention it would have been obvious to a person of ordinary skill in the art to add flash memory to store a plurality of supply voltages, as taught by Schutz to the microprocessor as taught by Dischler. The motivation for doing so would have been to increase circuit performance by avoiding speed limiting voltage/temperature combinations [Column 6, lines 35-37].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nirav Amin whose telephone number is (703) 305-8649. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NA


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